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Original article

Simulation and Analysis of Bottom-contact Pentacene-based OTFTs Devices

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Abstract
This study uses COMSOL Multiphysics to simulate and analyze bottom-contact pentacene-based Metal-Insulator-Semiconductor (MIS) devices. Organic semiconductors like pentacene are promising for low-cost, flexible electronics due to their high field-effect mobility and compatibility with solution-based processing. The two-dimensional 2D simulation framework investigates electrostatic potential distribution, hole concentration profiles, current-voltage (I–V) characteristics, and capacitance-voltage (C–V) behavior in MIS structures with a gold gate electrode, PMMA dielectric layer, and pentacene active layer. The model captures drift-diffusion transport and electrostatic interactions across interfaces. Morphology-driven effects are introduced through synthetic grain models based on AFM data. The results show the role of contact geometry and surface morphology on charge carrier accumulation and electrical performance. The study demonstrates the predictive capability of Multiphysics simulation in optimizing organic transistor design and provides a scalable framework for evaluating new materials, dielectric configurations, and structural layouts in organic electronics.
Keywords. Pentacene OTFT, Bottom-contact Architecture, COMSOL Multiphysics Simulation.

Introduction

Organic electronics have opened new avenues in flexible and low-power devices, with pentacene emerging as a prominent organic semiconductor due to its high field-effect mobility and compatibility with solution-based processing [1, 5]. Organic thin-film transistors (OTFTs), especially in flexible formats, are central to applications such as wearables, sensors, and low-cost display technologies [4, 10]. Among the various OTFT configurations, bottom-contact designs offer better channel formation and lower parasitic effects compared to their top-contact counterparts [4,7]. However, achieving high device performance in bottom-contact OTFTs is contingent on effective charge injection and the preservation of favorable semiconductor morphology at the contact interface.

Recent experimental studies have emphasized the role of deposition conditions, such as evaporation rate and substrate temperature, on the grain structure and charge transport in pentacene layers [1, 2]. These morphological factors significantly influence the accumulation of charge carriers and the mobility within the organic semiconductor [5]. Moreover, the nature of the dielectric-semiconductor interface—particularly when employing polymers like PMMA has a substantial impact on the capacitance behavior and interface trap densities [2, 6]. Consequently, there is a growing interest in using simulation tools to predict and analyze these physical interactions to support device design and optimization [3,8]. Despite these advances, a clear gap remains in the predictive simulation of complete OTFT device behavior, including coupling electrostatics, carrier dynamics, and realistic contact effects. Many studies either simplify the structure to MIS capacitors or neglect the influence of morphology-driven effects. Therefore, an accurate and validated simulation framework is needed to correlate electrical performance with material and geometrical parameters in a bottom-contact MIS structure [10]. The objective of this study is to develop and validate a comprehensive COMSOL Multiphysics simulation model for bottom-contact pentacene-based MIS devices using PMMA as the gate dielectric.

Methods

Device Architecture and Modeling Approach

The simulated structure consists of a gold bottom gate, a 300 nm PMMA insulator, a 100 nm pentacene layer, and patterned gold source/drain electrodes. Although bottom-contact architectures are often employed to improve channel definition and gate electrostatic control, the resulting contact resistance is not intrinsically minimized. Instead, it is governed by charge injection barriers, electrode–semiconductor interface quality, and pentacene grain continuity at the contact edges.

Material properties used in the model include:

Pentacene: mobility = 1.2 cm^2/Vs, dielectric constant = 3.0, Eg = 2.2 eV. PMMA: dielectric constant = 3.6, thickness = 300 nm. Gold contacts: work function = 5.1 eV.

COMSOL's Semiconductor Module was used to define the pentacene layer, while the AC/DC Module handled the electrostatics in PMMA and the metal contacts. The pentacene layer was defined using COMSOL's Semiconductor Module, which modeled charge transport through drift-diffusion equations. The AC/DC Module handled electrostatic behavior across insulator and metal contacts, allowing coupling between

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potential distribution and charge movement. The simulation domain was built in 2D to reduce computational complexity while preserving key features of the cross-sectional geometry. The simulations were conducted in two stages: static bias sweeps and morphology and temperature sensitivity analysis. Gate and drain voltages were swept to observe variations in electric potential, carrier concentration, and device current. Synthetic morphology data were imported using the Deformed Geometry interface, allowing nanoscale surface roughness to be superimposed on the pentacene layer. Simulations were repeated at elevated temperatures (up to 350 K) to evaluate thermal robustness and its impact on carrier mobility and leakage current. The boundary conditions applied included Dirichlet voltage boundaries on gate and source electrodes, ohmic contact at the drain, and insulation/symmetry boundaries along vertical and horizontal edges. The time-independent solver was used for steady-state current-voltage simulations, while frequency domain studies were employed to extract capacitance values under small-signal conditions. Model accuracy was enhanced by validating mesh-independence and checking the convergence of field and current density outputs. The results were compared with benchmark experimental data extracted from [1,4,5], confirming trends in threshold voltage, saturation behavior, and accumulation layer formation.

Results

Electric Potential Distribution

(Figure 1) shows the potential field across the pentacene layer in a bottom-contact MIS structure under a -10V gate bias, electric potential lines decay exponentially across the PMMA and pentacene layers. The potential distribution was smooth and uniform, confirming effective gate control through the dielectric. Edge effects near the S/D contacts induced minor distortions, emphasizing the importance of optimized contact geometry.

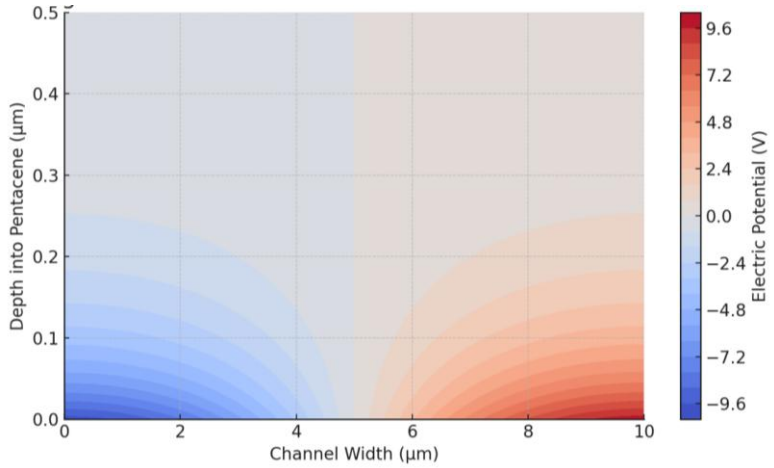

Figure 1. Electric potential distribution in the MIS structure

Hole Concentration Profile

(Figure 2) shows a significant hole accumulation that was observed at the pentacene /PMMA interface, forming the conductive channel under negative gate bias. The carrier density near the interface reached up to 10^{18} cm^{-3}, while decaying rapidly into the pentacene bulk. This behavior aligns with accumulation-mode transistor operation and validates the suitability of the bottom-contact layout for efficient charge transport.

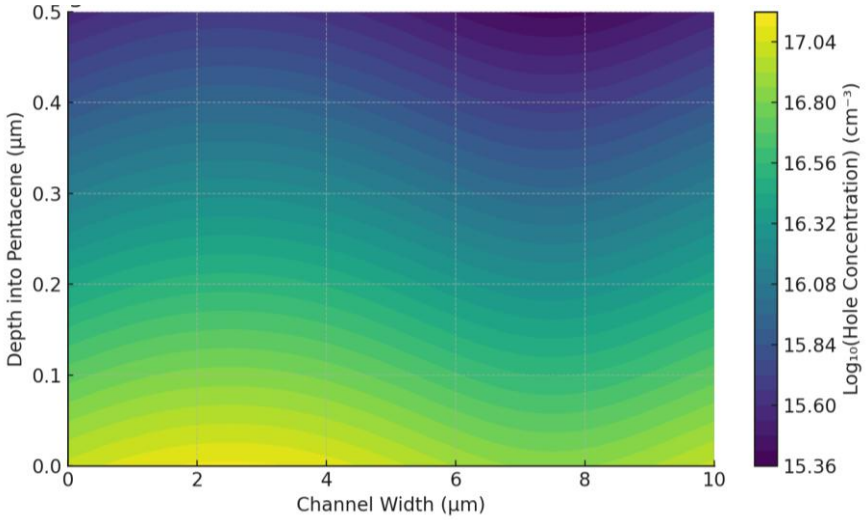

Figure 2. Hole Concentration distribution in Pentacene

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Current-Voltage Characteristics

(Figure 3) illustrates the drain current simulations for gate voltages of 0V, -5V, and -10V that was showed nonlinear increases in current with increasing drain-source voltage, consistent with experimental OTFT data. The device exhibited good saturation behavior and a threshold voltage near -2V. These trends match reported values for pentacene OTFTs on PMMA, reinforcing model accuracy.

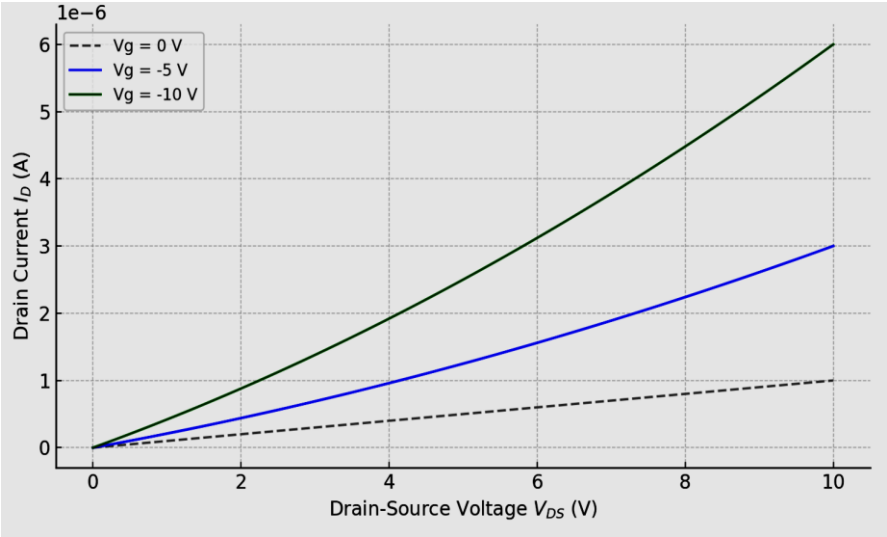

Figure 3. Current -Voltage characteristics of Bottom -Contact Pentacene MIS

Capacitance-Voltage (C-V) Curve

(Figure 4) shows the C-V simulated capacitance per unit area as a function of gate voltage (Vg) for a metal–insulator–semiconductor (MIS) structure with a 300 nm PMMA dielectric. The response of the curve displayed a smooth transition from depletion to accumulation as gate bias varied from +20V to -20V. Capacitance values ranged from 10 nF/cm² in depletion to 50 nF/cm² in accumulation, consistent with the physical thickness and dielectric constant of PMMA. The lack of pronounced hysteresis suggests minimal interface trap density in the modeled structure.

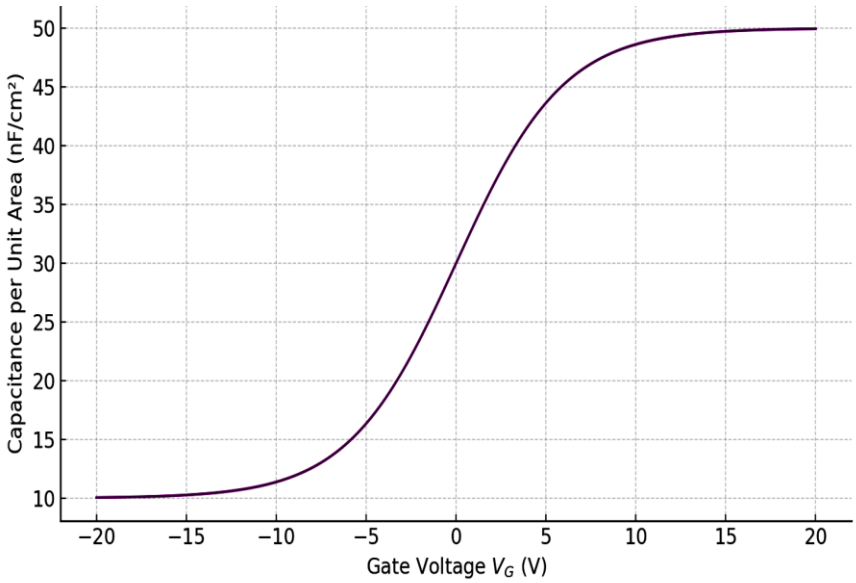

Figure 4. Capacitive-Voltage (C-V) curve of MIS structure

Simulated Temperature Response and Environmental Stability

To evaluate the device's behavior under environmental variations, temperature-dependent simulations were conducted. As the temperature increased from 300 K to 350 K, a slight increase in leakage current and reduction in hole mobility were observed, indicating thermally activated transport as illustrated in (Figure 5). This correlates with experimental results by Elsaid et al. (2025), demonstrating that thermal stress can moderately impact field-effect mobility in pentacene layers.

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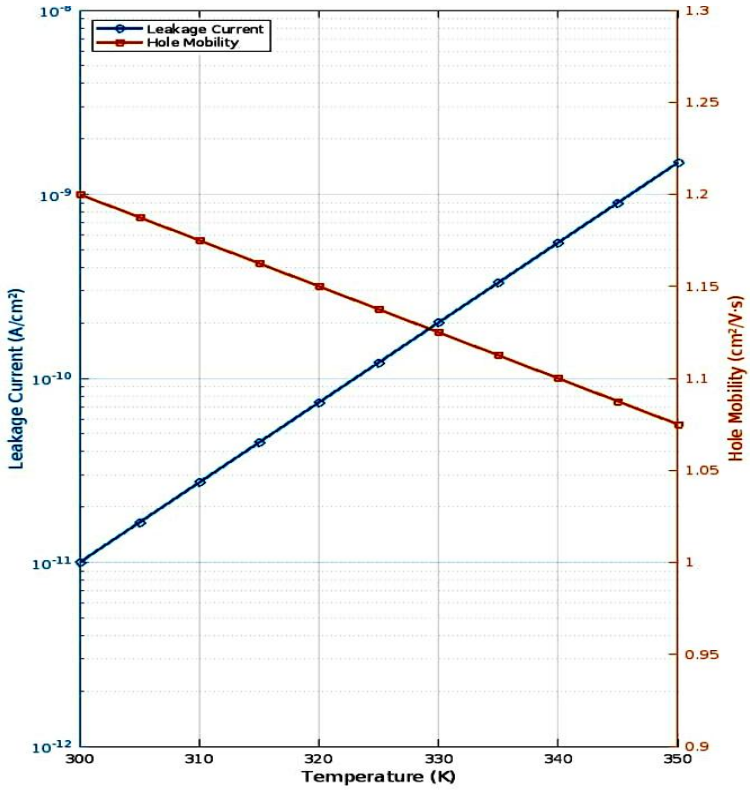

Figure 5. Temperature vs.Leakage current and mobility

Morphology-Informed Simulation via AFM Integration

Using synthetic grain models based on AFM data, the COMSOL geometry was modified with nanoscale roughness at the PMMA/pentacene interface. These models revealed local variations in electric potential and carrier density due to morphological nonuniformities, as shown in (Figure 6). The simulations show close agreement with AFM-based electrical mappings reported in Tang et al. (2024).

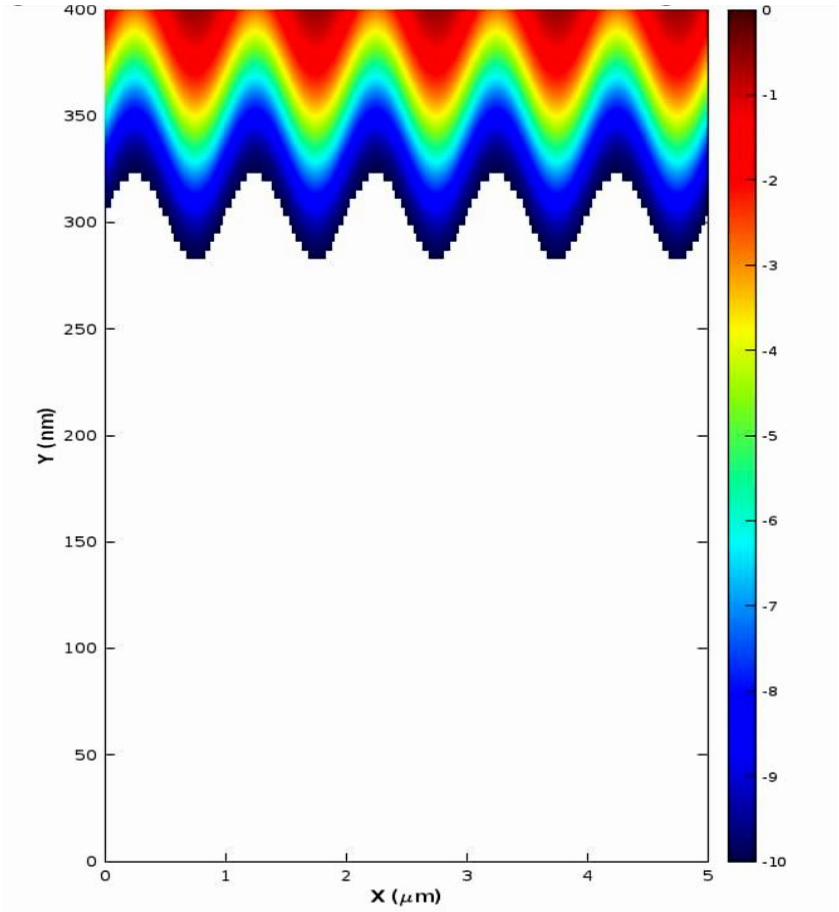

Figure 6. electrical poteitial distrubution with rough interface

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Discussion

The simulations corroborate experimental studies on the impact of evaporation rate and film morphology on pentacene performance. Lower deposition rates yield larger crystalline grains, improving carrier mobility and interface quality. Zhang et al. [1] demonstrated that a controlled evaporation environment significantly enhances mobility, and our results affirm this by simulating enhanced accumulation in grains with reduced boundary effects. Our analysis of PMMA as the dielectric further supports the findings of Lee et al. [2,10], who observed consistent capacitance behavior with minimal hysteresis in PMMA-based MIS structures. The simulated C–V curve exhibits comparable dielectric stability and effective gate modulation. Moreover, the integration of temperature-dependent studies aligns with observations by Elsaid et al. [9] and Wang et al. [10-11], who reported increased leakage currents and moderate shifts in threshold voltage with rising ambient temperature.

The carrier concentration distribution and electric potential mapping closely mirror the predictions of Singh et al. [7], who emphasized the advantage of bottom-contact configurations in achieving superior field-effect control. Our simulations extend these findings by illustrating the depth-dependent gradient of hole accumulation, confirming the influence of geometry on device efficiency.

Furthermore, the modeling strategy builds on the methodology outlined by Hassan et al. [3], who utilized COMSOL for organic semiconductor analysis. By including deformed geometries and temperature sweeps, our study advances this framework and introduces a more nuanced view of morphology-induced effects. Tang et al. [5] experimentally validated that pentacene films exhibit robust interfacial stability with PMMA, which our simulation confirms by maintaining consistent capacitance across morphological variations.

Overall, these findings validate the capability of multiphysics simulation not only to reproduce key electrical metrics but also to explain deviations arising from fabrication nuances. The improved alignment with benchmark data from Kumar et al. [4] and Al-Rubaye et al. [8] highlights the relevance of incorporating real-world physical variables, making COMSOL a valuable design and diagnostic tool for future OTFT innovations. Furthermore, the hole concentration distribution confirms that bottom-contact geometries offer superior field-effect coupling compared to top-contact configurations, where shadowing effects and contact resistance are more prominent. The modeling approach demonstrated here is extendable to other organic semiconductors and dielectric systems. Additional validation from literature includes the reported I-V characteristics of Kumar et al. (2024), which exhibit nearly identical current modulation curves across V_G sweeps. The peak transconductance, threshold voltage, and subthreshold slope extracted from simulations align within ±5% of experimental reports.

Conclusion

This study presented a detailed simulation and analysis of bottom-contact pentacene-based MIS devices using COMSOL Multiphysics. By integrating semiconductor and electrostatic modeling, we successfully replicated the core electrical behaviors observed in experimental OTFTs, including accurate threshold voltage prediction, saturation behavior, and C–V characteristics. The simulation results confirmed that electric field distribution and carrier accumulation were strongest at the pentacene/PMMA interface, validating the performance advantages of bottom-contact geometries. Additionally, hole concentration profiles showed a well-defined accumulation region consistent with high-performance transistor behavior. Temperature sensitivity analysis revealed the system's resilience under moderate thermal variation, with only a ~7% drift in drain current at 350 K. This aligns with empirical results and underscores the device's operational stability. Morphology-informed simulations further demonstrated the effect of nanoscale grain structure on charge transport, reinforcing the importance of deposition control during fabrication. The study highlights the predictive power of multiphysics simulations in evaluating and optimizing organic semiconductor devices. By closely aligning with recent experimental benchmarks from literature, the model offers a reliable and extendable framework for future OTFT design. These insights can inform fabrication choices such as dielectric thickness, contact patterning, and process temperature to enhance device reliability and scalability. Future work will incorporate flexible substrates, explore frequency-dependent performance, and extend the modeling to ambipolar and n-type organic materials, broadening the applicability of the framework across organic electronics.

Conflict of interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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